Atty. Dkt. No.: 039153/0684 (H1719)

U.S. PATENT APPLICATION

for

A METHOD OF FABRICATING A STRAINED SILICON CHANNEL FINFET

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CROSS REFERENCE TO RELATED APPLICATIONS

The present application is related to United States Patent Application No. _____, filed on ____ by Goo et al. and entitled "REPLACEMENT GATE FINFET PROCESS" (Atty. Dkt. No. 039153/0680); United States Patent Application No. 10/237,829, filed on September 9, 2002 by Tabery et al. and entitled "PLANAR FINFET PATTERNING USING AMORPHOUS CARBON" (Atty. Dkt. No. 039153/0628); and United States Patent Application No. 60/415,226, filed on September 30, 2002 by Goo et al. and entitled "FINFET HAVING IMPROVED CARRIER MOBILITY AND METHOD OF ITS FORMATION" (Atty. Dkt. No. 039153/0657), all of which are assigned to the Assignee of the present application.

FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuits (ICs) and methods of manufacturing integrated circuits. More particularly, the present invention relates to a method of fabricating integrated circuits having transistors with a fin-shaped channel region or FinFETS.

BACKGROUND OF THE INVENTION

[0002] Integrated circuits (ICs), such as ultra-large-scale integrated (ULSI) circuits, can include as many as one million transistors or more. The ULSI circuit can include complementary metal oxide semiconductor (CMOS) field effect transistors (FETS). Such transistors can

include semiconductor gates disposed above a channel region and between source and drain regions. The source and drain regions are typically heavily doped with a P-type dopant (e.g., boron) or an N-type dopant (e.g., phosphorous).

[0003] As transistors become smaller, it is desirous to increase the charge carrier mobility in the channel region. Increasing charge carrier mobility increases the switching speed of the transistor. Channel regions formed from materials other than silicon have been proposed to increase charge carrier mobility. For example, conventional thin film transistors which typically utilize polysilicon channel regions have been formed on a silicon germanium (Si-Ge) epitaxial layer above a glass (e.g., SiO_2) substrate. The Si-Ge epitaxial layer can be formed by a technique in which a semiconductor thin film, such as an amorphous silicon hydride (a-Si:H), an amorphous germanium hydride (a-Ge:H), or the like is melted and crystallized utilizing irradiation of pulse laser beams.

[0004] In a bulk type device, such as a metal oxide semiconductor field effect transistor (MOSFET), the use of Si-Ge materials can be used to increase charge carrier mobility, especially for hole-type carriers. A tensile strained silicon channel region, such as a silicon channel containing germanium, can have carrier mobility 2-5 times greater than a conventional Si channel region due to reduced carrier scattering and due to the reduced mass of holes in the germanium-containing material. According to conventional Si-Ge formation techniques for bulk-type devices, a dopant implant molecular beam epitaxy (MBE) technique forms a Si-Ge epitaxial layer. However, the MBE technique requires very complicated and expensive equipment, and is not feasible for mass production of ICs.

[0005] Double gate transistors, such as vertical double gate silicon-on-insulator (SOI) transistors or FinFETS, have significant advantages related to high drive current and high immunity to short channel effects. An article by Huang, et al. entitled "Sub-50 nm FinFET: PMOS" (1999 IEDM) discusses a silicon transistor in which the active layer is surrounded by a gate on two sides. However, double gate structures can be difficult to manufacture using conventional IC fabrication tools and techniques. Further, patterning can be difficult because of the topography associated with a silicon fin. At small critical dimensions, patterning may be impossible.

[0006] By way of example, a fin structure can be located over a layer of silicon dioxide, thereby achieving an SOI structure. Conventional FinFET SOI devices have been found to have a number of advantages over devices formed using semiconductor substrate construction, including better isolation between devices, reduced leakage current, reduced latch-up between CMOS elements, reduced chip capacitance, and reduction or elimination of short channel coupling between source and drain regions. While the conventional FinFET SOI devices provide advantages over MOSFETs formed on bulk semiconductor substrates due to its SOI construction, some fundamental characteristics of the FinFET, such as carrier mobility, are the same as those of other MOSFETs because the FinFET source, drain and channel regions are typically made from conventional bulk MOSFET semiconductor materials (e.g., silicon).

[0007] The fin structure of FinFET SOI devices can be located below several different layers, including a photoresist layer, a bottom anti-reflective coating (BARC) layer, and a polysilicon layer. Various problems can exist with such a configuration. The photoresist layer may be thinner over the fin structure. In contrast, the polysilicon layer may be very thick at

the edge of the fin structure. The BARC may be thick at the edge of the fin structure. Such a configuration leads to large over-etch requirements for the BARC layer and the polysilicon layer. Such requirements increase the size of the transistor.

[0008] When manufacturing FinFET structures, it is desirous to have a fin channel structure with a high aspect ratio. A higher aspect ratio for the fin channel structure allows a larger amount of current to be provided through the same amount of topographical area. Heretofore, fabrication of high aspect ratio FinFETS has not been practicable for large-scale fabrication.

[0009] Thus, there is a need for an integrated circuit or electronic device that includes channel regions with higher channel mobility, higher immunity to short channel effects, and higher drive current. Further, there is a need for a method of patterning FinFET devices having small critical dimensions. Even further, there is a need for a method of fabricating strained silicon fin-shaped channels for FinFET devices. Yet further, there is a need for a high aspect ratio FinFET device. Even further still, there is a need for an efficient method of manufacturing a high aspect ratio fin structure. Further still, there is a need for a FinFET device with a strained semiconductor fin-shaped channel region. Yet even further, there is a need for a process of fabricating a FinFET device with a strained semiconductor fin-shaped channel.

SUMMARY OF THE INVENTION

[0010] An exemplary embodiment relates to a method of forming a fin-shaped channel region. The method includes providing a

compound semiconductor layer above an insulating layer and providing a trench in the compound semiconductor layer. The method also includes providing a strained semiconductor layer above the compound semiconductor layer and within the trench. The trench is associated with the fin-shaped channel region. The method further includes removing the strained semiconductor layer from above the compound semiconductor layer and removing the compound semiconductor layer to leave the strained semiconductor layer and form the fin-shaped channel region. When the strained semiconductor layer is removed, the strained semiconductor layer is left within the trench.

[0011] Another exemplary embodiment relates to a method of FinFET channel structure formation. The method includes providing a first layer above an insulating layer above a substrate and providing an aperture in the first layer. The first layer includes silicon and germanium and the aperture extends to the insulating layer. The method also includes providing a strained material within the aperture and removing the first layer to leave the strained material.

[0012] Yet another exemplary embodiment relates to a method of fabricating an integrated circuit including a fin-based transistor. The method includes steps of providing an insulative material, providing a strain inducing layer above the insulative material, and providing an aperture in the strain inducing layer. The method further includes forming a strained material in the aperture by selective epitaxial growth, removing at least a portion of the strain inducing layer to thereby leave the strained material as a fin structure and providing a gate structure for the fin structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Exemplary embodiments will hereafter be described with reference to the accompanying drawings, wherein like numerals denote like elements, and:

[0014] FIGURE 1 is a flow diagram depicting exemplary operations in a process for forming a fin-based transistor for an integrated circuit in accordance with an exemplary embodiment;

[0015] FIGURE 2 is a general schematic planar top view representation of a portion of an integrated circuit fabricated according to the process shown in FIGURE 1 in accordance with an exemplary embodiment;

[0016] FIGURE 3 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 2 taken across line 3-3 in accordance with an exemplary embodiment;

[0017] FIGURE 4 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 2 taken across line 4-4 in accordance with an exemplary embodiment;

[0018] FIGURE 5 is a schematic cross-sectional view representation of a portion of the integrated circuit illustrated in FIGURE 3 showing an insulating layer above a substrate for use in the process illustrated in FIGURE 1;

[0019] FIGURE 6 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 5 showing a compound semiconductor deposition operation;

[0020] FIGURE 7 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 6 showing a trench formation operation;

[0021] FIGURE 8 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 7 showing an epitaxial growth operation;

[0022] FIGURE 9 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 8 showing a chemical mechanical polish operation;

[0023] FIGURE 10 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 9 showing a selective etching operation;

[0024] FIGURE 11 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 5 showing a gate oxide formation operation;

[0025] FIGURE 12 is a flow diagram depicting exemplary operations in another process for forming a fin-based transistor for an integrated circuit in accordance with an exemplary embodiment;

[0026] FIGURE 13 is a general schematic planar top view representation of a portion of another integrated circuit fabricated according to the process illustrated in FIGURE 12 in accordance with another exemplary embodiment;

[0027] FIGURE 14 is a schematic cross-sectional view representation of the portion of the integrated circuit illustrated in FIGURE 13

taken across line 14-14 in accordance with an exemplary embodiment and showing a masking operation for the process illustrated in FIGURE 12;

[0028] FIGURE 15 is a flow diagram depicting exemplary operations in yet another process for forming a fin-based transistor for an integrated circuit in accordance exemplary embodiment;

[0029] FIGURE 16 is a schematic cross-sectional view representation of a portion of the integrated circuit fabricated according to the process shown in FIGURE 15 showing a spacer material provision operation; and

[0030] FIGURE 17 is a schematic cross-sectional view representation of a portion illustrated in FIGURE 16 showing a spacer material removal operation to leave spacers in an aperture.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0031] FIGURE 1 is a flow diagram depicting exemplary operations in a method or process 10 of patterning a fin-based transistor or fin field effect transistor (FinFET). The flow diagram illustrates by way of example some operations that may be performed. Additional operations, fewer operations, or combinations of operations may be utilized in various different embodiments. Flow diagram 110 (FIGURE 12) illustrates on alternative embodiment in which a masking step is used to protect source and drain locations during etching. Flow diagram (FIGURE 15) illustrates another alternative embodiment in which a spacer is utilized to increase the aspect ratio of the fin structure.

[0032] In FIGURE 1, a wafer including a compound semiconductor layer over an insulative layer is provided in a step 15. The wafer can be purchased or manufactured using SIMOX (oxygen implementation into silicon and annealing or wafer bonding). In a step 25, the compound semiconductor layer is patterned to form a channel trench. In a step 45, a semiconductor layer is formed above the compound semiconductor and in the trench. The trench in the compound semiconductor layer preferably has a bottom which reaches a top surface of the insulative layer.

[0033] In a step 55 of process 10, the semiconductor layer is planarized above the compound semiconductor layer, thereby removing it from a top surface of the compound semiconductor layer and leaving it within the trench. In a step 65, the compound semiconductor layer is removed, thereby leaving a fin-shaped channel structure or region above the insulative layer. In a step 75, a gate structure is provided to complete a fin-based transistor.

[0034] With reference to FIGURES 2-4, process 10 is utilized to form a portion of an integrated circuit 100 that includes a fin-based transistor or FinFET. FIGURES 2-11, 13, 14 and 16-17 are not drawn to scale. FIGURES 3 and 4 are drawn to show the high aspect ratio associated with fin-shaped channel region 152. However, the remaining figures are not drawn to highlight the high aspect ratio for drawing efficiency. It is noted that FIGURES 1-10 are provided to schematically illustrate and they are not proportional engineering drawings. In FIGURE 2, a top view shows a source region 22 and a drain region 24 on opposite sides of a fin-shaped channel region 152. A gate conductor 166 is provided over channel region 152 and a gate dielectric layer 160 which is provided on three sides of channel region

152. As seen in FIGURE 3, gate conductor 166 has a U-shaped cross-sectional shape and can surround three sides of fin-shaped channel region 152. Gate conductor 166 can be a metal layer or can be a polysilicon layer (e.g., a doped polysilicon layer). Alternatively, conductor 166 can be provided only adjacent lateral sides 163 of channel region 152.

[0035] Dielectric layer 160 can be made of any suitable material for use in gate structures. Dielectric layer 160 can have a U-shaped cross-sectional shape and can be underneath conductor 166. In one embodiment, dielectric layer 160 is thermally grown silicon dioxide. In another embodiment, dielectric layer 160 is a high-K gate dielectric layer, a silicon nitride layer, or another insulator. Layers 160 and gate conductor 166 form a gate structure on lateral sides 163 and above a top surface 167 of fin-shaped channel region 152. Channel region 152 can be subjected to tensile strain through epitaxial growth seeded from a compound semiconductor layer, such as a silicon germanium layer.

[0036] In FIGURE 4, source region 22 and drain region 24 are covered by dielectric layer 160 on all sides. In another embodiment, layer 160 only covers channel region 152 and is provided only under gate conductor 166. As shown in FIGURE 2, gate conductor 166 does not overlap source and drain regions 22 and 24. However, gate conductor 166 can be provided to borders 32 and 34 and even overlap borders 32 and 34 if proper isolation is provided.

[0037] Advantageously, fin-shaped channel region 152 has a relatively high aspect ratio. Preferably, region 152 has a height of between approximately 20nm and 120nm (e.g., a thickness) and a width of between approximately 5nm and 20nm. The fin width is determined by minimum

transition gate length (1/3 to 1/2 of the gate length). In one embodiment, the aspect ratio is between approximately 4 and 6. High aspect ratios associated with region 152 provide a high current transistor through a relatively small area.

[0038] Preferably, fin-shaped channel region 152 is a tensile-strained silicon material manufactured in accordance with process 10, process 110, or process 210. Conductor 166 can have a thickness of between approximately 500Å and 100Å and gate dielectric layer 160 can have a thickness of between approximately 10Å and 50 Å. Although shown in FIGURES 2-4, channel region 152 can be utilized with a variety of different types of gate structures. Gate conductors 166 and dielectric layer 160 are not shown in a limiting fashion.

[0039] Preferably, the length (from top to bottom in FIGURE 2) from an end of source region 22 to an end of drain region 24 is between approximately .5 and 1 micron and a width (from left to right of channel region 152 in FIGURE 2) of source and drain regions 24 is between approximately .2 and .4 micron. Source region 22 and drain region 24 include a strained silicon material, a single crystalline material, or a compound semiconductor material. In one embodiment, regions 22 and 24 are made of the same material as region 152. Regions 22 and 24 are preferably doped with N-type or P-type dopants to a concentration of 10^{14} to 10^{20} dopants per cubic centimeter.

[0040] Fin-shaped channel region 152 is provided above an insulative layer 130. Insulative layer 130 is preferably a buried oxide structure, such as, a silicon dioxide layer. In one embodiment, layer 130 has

a thickness of between approximately 2000 – 2000Å. Layer 130 can be provided above any type of substrate or may be a substrate itself.

[0041] In one embodiment, insulative layer 130 is provided above a semiconductor base layer 150 such as a silicon base layer. Layers 130 and 150 can comprise a silicon or semiconductor-on-insulator (SOI) substrate. Alternatively, fin-shaped channel region 152 can be provided above other types of substrates and layers. However, the preferred embodiment provides channel region 152 above an insulating layer such as a buried oxide layer (BOX) above a silicon substrate.

[0042] The transistor associated with regions 22 and 24 can have a barbell shape having large pad regions for drain region 22 and source region 24. Alternatively, the transistor can be simply bar shaped. The orientation shown in FIGURE 2 is not disclosed in the limiting fashion.

[0043] In FIGURE 5, a substrate is provided including layers 150 and 130. In FIGURES 5-11, the various layers and structures are not drawn according to scale and do not include the large height associated with FIGURES 3-4. In FIGURE 6, a layer 140 is provided above layer 130 in accordance with step 15 of process 10 (FIGURE 1). In one embodiment, layer 140 can be deposited by a chemical vapor deposition (CVD) above insulative layer 130. Alternatively, layers 130, 140 and 150 can be provided as an SOI substrate in which layer 140 includes silicon germanium.

[0044] Layer 140 is preferably a compound semiconductor layer or a strain-inducing semiconductor layer such as a silicon germanium layer. Layer 140 is preferably a composition of $Si_{1-x}Ge_x$, where X is approximately 0.2, and is more generally in the range of 0.1 to 0.3. Various methods can be utilized to produce layers 140, 130, and 150. Layer 140 is

preferably provided as a 20nm to 120nm thick layer and induces strain in subsequently formed region 152.

[0045] In FIGURE 7, an aperture or trench 142 is provided in layer 140 in accordance with step 25 of process 10 (FIGURE 1). Preferably, trench 142 has a bottom coplanar with a top surface 143 of layer 130. Alternatively, the bottom of trench 142 can terminate before layer 130. Various dimensions can be utilized for trench 142 depending upon design criteria and system parameters for the fin-based transistor.

[0046] In one embodiment, trench 142 has a height of 20 – 120nm and a width of between approximately 5 and 20nm. Trench 142 is generally associated with the dimensions of fin-shaped channel region 152. Further, trench 142 can have a length (into and out of the page associated with FIGURE 7) of between approximately 1.0 micron to 1.5 micron and 1 micron.

[0047] In one embodiment, trench 142 is formed in a photolithographic process. In one such process, antireflective coatings, hard masks, and photoresist materials are utilized to pattern a layer or layers above layer 140. The patterned layer or layers are used to selectively etch layer 140 to create trench 142.

[0048] In FIGURE 8, a layer 144 is formed above layer 140 in step 45 of process 10 (FIGURE 1). Preferably, layer 144 fills the entirety of trench 142. Layer 144 is preferably a 40 – 240nm thick layer formed by a growth process. In one preferred embodiment, layer 144 is formed by selective silicon epitaxial growth using silane, disilane, and/or dichlorosilane, (using CVD or MBE).

[0049] Layer 144 is a strained layer due to the compound semiconductor layer (silicon germanium nature) of layer 140. Sidewalls of trench 142 serve as a seed for crystalline growth of layer 144. The silicon germanium lattice associated with layer 140 results in a more widely spaced interstitial silicon lattice in layer 144, thereby creating a tensile strain in layer 144. As a result, the epitaxial silicon associated with layer 144 is subject to tensile strain.

[0050] The application of tensile strain to layer 144 causes 4 of 6 silicon valance bands associated with the silicon lattice to increase in energy and 2 of its valance bands to decrease in energy. As a result of quantum effects, electrons effectively weigh approximately 30% less when passing through the lower energy bands of the strained silicon in layer 144. As a result, carrier mobility is dramatically increased in layer 144, offering the potential increase in mobility of 80% or more for electrons and 20% or more for holes. The increase in mobility has been found to persist for current fields of up to 1.5 megavolts/centimeters. These factors are believed to enable a device speed increase of 35% without further reduction of size, or 25% reduction in power consumption without a reduction in performance.

[0051] In FIGURE 9, layer 144 is subject to a removal step in a step 55 of process 10 (FIGURE 1). In one embodiment, a chemical mechanical polish can be utilized to remove all of layer 144 from directly above layer 130. The nature of the CMP operation allows layer 144 to remain in aperture or trench 142 to form channel region 152. Alternatively, or etching process can be utilized to remove layer 144.

[0052] Preferably, the CMP process is stopped so that layer 144 has a height of between approximately 20 and 120nm from a bottom of trench 142 to a top surface 153.

[0053] In FIGURE 10, layer 140 is removed in accordance with step 165 of process 10 (FIGURE 1). Preferably, layer 140 is removed in a dry etching technique selective to the material of layer 140. In one embodiment, the dry etching technique is selective to silicon germanium with respect to silicon. Layer 140 can be removed by a wet or an isotropic etch. The etching technique is not as selective to layer 144, thereby leaving fin-shaped channel region 152. Alternatively, etching techniques can be utilized to remove layer 140.

[0054] In FIGURE 11, a gate dielectric layer 160 is formed in accordance with step 175 of process 10 (FIGURE 1). Layer 160 can be thermally grown or deposited to a thickness of between approximately 10 and 50Å on the three exposed sides of channel region 152. In FIGURES 3 and 4, layer 165 is provided to complete the gate structure. Layer 165 can be a 500 to 1000Å thick polysilicon layer deposited by CVD.

[0055] With reference to FIGURE 12, process 110 is similar to process 10 in which steps having the same last two digits are essentially the same. However, process 110 includes a step 165 of removing compound layer 140 in accordance with a source/drain mask. Step 165 can be performed instead of step 65 in process 10 (FIGURE 1).

[0056] With reference to FIGURES 13 and 14, in step 165 of process 110, a mask 134 protects source and drain regions 22 and 24 during step 165. In one embodiment, source region 22 and drain region 24 are manufactured from layer 140, thereby providing silicon germanium

material for maintaining tensile stress on channel region 152. In this manner, mask 134 prevents layer 140 from being removed at the end points (regions 22 and 24 of the fin-shaped transistor). Alternatively, regions 22 and 24 can be material associated with layer 144 which are protected by mask 134. Mask 134 can be a photolithographic mask, a hard mask, or other suitable material. In one embodiment, mask 134 is a silicon dioxide or silicon nitride material.

[0057] In FIGURE 14, the various layers and structures are not drawn according to scale and do not include the large height associated with FIGURES 3-4. In addition, a bar shaped rather than bar-bell shaped transistor is shown in FIGURES 13-14.

[0058] With reference to FIGURE 15, process 210 is similar to processes 10 and 110 in which having the same last two digits are essentially the same. However, process 210 includes a step 227 in which a spacer material is grown within the transformed in step 225 to narrow the width of the trench. Such a step allows a higher aspect ratio for the fin-shaped channel region 152 to be built. Step 227 can be performed after steps 25 and 125 and before steps 45 and 145 in processes 10 and 110, respectively.

[0059] The spacer material can be a compound semiconductor layer, and can be the same material as used for layer 140. The spacer material can be selectively grown within trench 142 or grown across a top surface of layer 140 as well as within trench 142 and then selectively removed.

[0060] With reference to FIGURES 16 and 17, step 227 of process 210 is discussed below. FIGURE 16 and 17 are not drawn to scale

and do not include the large height associated with FIGURES 3-4. In this embodiment, step 227 forms a layer 151 of compound semiconductor material such as silicon germanium having the same ratio of germanium as layer 140. Layer 151 preferably grows on lateral side walls of trench 142 to thereby narrow the width of trench 142. Layer 151 is preferably an ultra thin layer.

[0061] Preferably, trench 142 has an original width of between approximately 5 and 100nm. The original width can be reduced by as much as approximately 10-30 percent or more by the use of layer 151.

[0062] In FIGURE 17, layer 151 is removed from a top surface of 140. Alternatively, layer 151 can remain and be removed in step 265 similar to steps 65 and 165 of processes 10 and 110. In one embodiment, layer 151 can be removed by chemical mechanical polish which removes all of layer 151 and a portion of 140. After step 227, process 210 continues similar to process 10 or process 110.

[0063] Layer 151 can be deposited by chemical vapor deposition growth, ALD or other technique as a conformal layer. The cross-sectional views of FIGURES 16 and 17 are shown in the same configuration as FIGURES 4-9.

[0064] It is understood that while the detailed drawings, specific examples, material types, thicknesses, dimensions, and particular values given provide a preferred exemplary embodiment of the present invention, the preferred exemplary embodiment is for the purpose of illustration only. The method and apparatus of the invention is not limited to the precise details and conditions disclosed. Various changes may be made

to the details disclosed without departing from the scope of the invention which is defined by the following claims.